Patent Claims

1. A method for converting a digital input value (Sq1) quantized according to a first quantization coefficient (Cq1) and encoded over and most n1 bits, into a digital output value (Sq2) quantized according to a second quantization coefficient (Cq2) and encoded over and most n2 bits, where n1 and n2 are nonzero integers, comprising the steps consisting in:

a) multiplying the digital input value (Sq1) by an integer B encoded over at most β bits, where β is a nonzero integer, in order to generate a first intermediate digital value (C) encoded over at most $n1+\beta$ bits;

b) fixed-point dividing said first intermediate digital value (C) by the number 2^{α}, where α is an integer less than or equal to $n1+\beta$, in order to generate said digital output value (Sq2),

wherein the number $\frac{B}{2^{\alpha}}$ is substantially equal to the ratio of said second quantization coefficient (Cq2) to said first quantization coefficient (Cq1);

and wherein step b) is carried out by means of a sigma-delta modulator.

2. The method as claimed in claim 1, wherein step b) comprises the steps consisting in:

b1) adding said first intermediate digital value (C), on the one hand, and a digital error value (E) encoded over at most α bits, on the other hand, in order to generate a second intermediate digital value (D) encoded over at most $n1+\beta+1$ bits;

b2) selecting the n2 most significant bits of said second intermediate digital value (D) as the digital output value (Sq2), where n2 is equal to $n1+\beta+1-\alpha$;

b3) selecting the α least significant bits of said second intermediate digital value (D) as the digital error value (E).

3. The method as claimed in claim 2, wherein step b2) and step b3) are carried out together with the aid of a discriminator for separating said $n1+\beta+1-\alpha$ most

significant bits of said second intermediate digital value (D), on the one hand, and said α least significant bits of said second intermediate digital value (D), on the other hand.

4. The method as claimed in claim 2, wherein step b2) is carried out via an operation of shifting to the right by α bits, which is applied to the $n1+\beta+1$ bits of the second intermediate digital value (D).

5. The method as claimed in claim 4, wherein step b3) is carried out by applying to the second intermediate digital value (D) a mask having at most $n1+\beta+1$ bits, the $n1+\beta+1-\alpha$ most significant bits of which are equal to the logical value 0 and the α least significant bits of which are equal to the logical value 1.

6. The method as claimed in claim 4, wherein step b3) is carried out, on the one hand, by an operation of shifting to the left by α, which is applied to the $n1+\beta+1-\alpha$ bits of the digital output value (Sq2) for generating a third intermediate digital value (F) encoded over at most $n1+\beta+1$ bits and, on the other hand, by a difference operation between said third intermediate digital value (F) and said first intermediate digital value (C).

7. The method as claimed in any one of the preceding claims, wherein neither the first quantization coefficient nor the second quantization coefficient is an integer multiple of the other.

8. A device for converting a digital input value (Sq1) quantized according to a first quantization coefficient (Cq1) and encoded over at most n1 bits, into a digital output value (Sq2) quantized according to a second quantization coefficient (Cq2) and encoded over at most n2 bits, where n1 and n2 are nonzero integers, comprising:

- multiplier means (10) for multiplying the digital input value (Sq1) by an integer B encoded over at most β bits, where β is a nonzero integer,

generating a first intermediate digital value (C) encoded over at most $n1+\beta$ bits;

- divider means for fixed-point dividing said first intermediate digital value (C) by the number 2^{α}, where α is an integer less than or equal to $n1+\beta$, generating said digital output value (Sq2),

wherein the number $\frac{B}{2^{\alpha}}$ is substantially equal to the ratio of said second quantization coefficient (Cq2) to said first quantization coefficient (Cq1);

and wherein said divider means comprise a sigma-delta modulator (20).

9. The device as claimed in claim 8, wherein the sigma-delta modulator (20) is a 1^{st} order to sigma-delta modulator.

10. The device as claimed in claim 9, wherein the sigma-delta modulator (20) comprises:

- adder means (21) which receive as input said first intermediate digital value (C) as a first operand, on the one hand, and a digital error value (E) encoded over at most α bits as a second operand, on the other hand, and which deliver as output a second intermediate digital value (D) encoded over at most $n1+\beta+1$ bits;

- selection means (23) for selecting the n2 most significant bits of said second intermediate digital value (D) as the digital output value (Sq2), where n2 is equal to $n1+\beta+1-\alpha$; and for selecting the α least significant bits of said second intermediate digital value (D) as the digital error value (E).

11. The device as claimed in claim 10, wherein said selection means (23) consist of a discriminator for separating said $n1+\beta+1-\alpha$ most significant bits of said second intermediate digital value (D), on the one hand, and said α least significant bits of said second intermediate digital value (D), on the other hand.

12. The device as claimed in claim 10, wherein said selection means (23) comprise an operator (24) for shifting to the right by α bits, which receives as

input the $n1+\beta+1$ bits of the second intermediate digital value (D), and which delivers as output the $n1+\beta+1-\alpha$ most significant bits of the second intermediate digital value (D) as a digital output value (Sq2).

13. The device as claimed in claim 12, wherein said selection means (23) further comprise means (25) for applying to the second intermediate digital value (D) a mask (M) having at most $n1+\beta+1$ bits, the $n1+\beta+1-\alpha$ most significant bits of which are equal to the logical value 0 and the α least significant bits of which are equal to the logical value 1, so as to select the α least significant bits of said second intermediate digital value (D) as the digital error value (E).

14. The device as claimed in claim 12, wherein said selection means (23) further comprise, on the one hand, an operator for shifting to the left by α bits, which receives as input the $n1+\beta+1-\alpha$ bits of the digital output value (Sq2) and delivers as output a third intermediate digital value (F) encoded over at most $n1+\beta+1$ bits and, on the other hand, a difference operator which receives said third intermediate digital value (F) as a first operand and said first intermediate digital value (C) as a second operand, and which delivers as output said digital error value (E).

15. The device as claimed in any one of claims 10 to 14, wherein the error signal (E) is delivered to the input of the adder means (21) through a unitary delay operator (22).

16. A digitally modulated frequency synthesizer, comprising a phase-locked loop (PLL) comprising a variable-ratio frequency divider (14) in the return path, wherein the division ratio is controlled by a digital value (Sc) obtained in particular from a real value (F_{ch}) corresponding to the central frequency of a radio channel, the synthesizer further comprising a conversion device (18) as claimed in any one of claims 8 to 15 for reducing the quantization error affecting said real value.